AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/347,690

Filing Date: July 2, 1999

Title: LOGIC VERIFICATION IN LARGE SYSTEMS

Assignee: Intel Corporation

Page 2 Dkt: 884.107US1 (INTEL)

IN THE SPECIFICATION

Please amend the paragraph in the specification that begins at page 7, line 10, as follows:

Figure 6 is a flow diagram of some embodiments of a method 600 of preparing a circuit model for simulation while reducing inter-partition communication in the simulation. Reducing the inter-partition communication time in a simulation allows the simulation to complete more quickly. Method 600 begins at start 603 and includes a grouping 606 operation, a reducing 609 operation, and terminates at end [[612]]615. Extended latch boundary components are partitioned according to different criteria. In one embodiment, in the grouping 606 operation, the extended latch boundary components are grouped to reduce the communication time within the plurality of partitions. This is accomplished by grouping in the same partition the extended latch boundary components that are tightly coupled. In another embodiment, the reducing 609 operation occurs after a simulation and groups in the same partition extended latch boundary components that demonstrate significant communication between partitions during the simulation. In still another embodiment, in the reducing 609 operation the communication time within the plurality of partitions to less than about ten percent of the total simulation time is achieved by adjusting the grouping of the extended latch boundary components.